UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,652	01/18/2002	Ronalf Kramer	1406/36	5317

25297 7590 10/17/2002

JENKINS & WILSON, PA
3100 TOWER BLVD
SUITE 1400
DURHAM, NC 27707

EXAMINER
TAN, VIBOL

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 10/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,652	KRAMER, RONALF	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because there is more than one paragraph. It should only be limited to a single paragraph. Correction is required. See MPEP § 608.01(b).

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "inverter delay device" in claim 3 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 4, and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Taguchi (U. S. PAT. 6,160,417).

In claim 1, Taguchi teaches all claimed features in Fig. 3, a circuit for generating an asynchronous signal pulse having a predetermined duration (a duty cycle) at an

output (DQ) of an integrated circuit (5), which has a first and a second transistor (13, 14) in the integrated circuit, which are connected in series between a supply potential (VCC) and ground (VSS=0V), firstly a control pulse (an output signal from 11 input into 13) having the predetermined duration (the duty cycle) being present at a control connection (at the gate of 13) of the first transistor (13) and then a control pulse (another output signal from 11 input into 14) being present at a control connection (at the gate of 14) of the second transistor (14), with the result that, for the predetermined duration, firstly the first transistor (13) and then the second transistor (14) is turned on and the connecting point (6) is firstly at the supply potential (VCC) and then at the ground (VSS=0V), and a resistor (30 or 31) for the definition of the active signal state, which is connected outside the integrated circuit (5) in parallel with one of the two transistors (13, 14) in the integrated circuit either between the supply potential (VCC) and the connecting point (6) or between the ground (VSS) and the connecting point (6).

In claim 4, Taguchi further teaches in Fig. 3, the circuit as claimed in claim 1, wherein the first transistor (13) is a P-channel MOS transistor and the second transistor (14) is an N-channel MOS transistor, the control connection (the gate electrode) of the first transistor (13) being inverted (PMOS transistor inherently having inverting gate electrode).

In claim 5, Taguchi further teaches in Fig. 3, the circuit as claimed in claim 4, wherein the first transistor (13) and the second transistor (14) form a CMOS inverter (12) with independent control gate connections (separate gate electrodes).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi in view of Proebsting (U. S. PAT. 5,926,050).

In claim 2, Taguchi teaches all claimed features, the circuit in claim 1 in Fig. 3 as described above; with the exception of disclosing a waiting time is provided between the first control pulse and the second control pulse, in which the two pulses do not overlap. However, Proebsting teaches in Figs. 4 and 5, a waiting time (t_{12}-t_{107}) is provided between the first control pulse (C2) and the second control pulse (F2), in which the two pulses do not overlap.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to apply a waiting time between the first control pulse and the second control pulse, in which the two pulses do not overlap, to ensure that one signal will arrive to condition a circuit before the other signal; and that the second transition of the second signal to arrive before that of the first signal.

In claim 3, Proebsting further teaches in Figs. 4 and 5 the circuit of claim 2, wherein one of the two control pulses (F2) is generated from the other of the two control pulses (C2) by an inverter delay device (64l).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to apply a waiting time between the first control pulse and the

second control pulse, in which the two pulses do not overlap, to ensure that one signal will arrive to condition a circuit before the other signal; and that the second transition of the second signal to arrive before that of the first signal.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Elachkar et al. teaches method and apparatus for testing an impedance-controlled input/output buffer in a highly efficient manner. Hesson teaches high speed CMOS driver circuit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (703) 306-5948. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-6251 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0959.

Vibol Tan

Patent Examiner, AU 2819